AN74170

PSoC® 1 Analog Structure and Configuration with PSoC Designer™

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Software Version: PSoC® Designer™ 5.1 or later
Related Application Notes: None

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AN74170 explains the analog structure of standard PSoC® 1 devices and how the global analog parameters affect many of the analog user modules.

Contents

Introduction

When designing with the PSoC 1 family of microcontrollers, you use PSoC Designer and its high-level interface to configure the PSoC, including the analog architecture. In addition to placing and configuring the individual user modules (building blocks), several global analog parameters also require configuration. Understanding these global parameters and the overall analog architecture is important, especially when a design consists of several analog user modules that are affected by these settings.

This application note assumes that you are familiar with the PSoC Designer development tool, and how to develop a project. Topics covered in this application note include the following:

- Analog PSoC block array structure
- Analog column structure
- Analog connectivity to GPIO pins
- Internal analog block interconnect
- Internal reference structure
- Global analog parameters
- Troubleshooting incorrect ADC operation

The devices covered in this application note include the PSoC devices intended for general-purpose applications that have a similar architecture as shown in Table 1. The PSoC devices intended solely for CapSense® (capacitive touch input) are not included in this application note, although some of the PSoC devices discussed do support CapSense.

Table 1 lists the analog resources for each part family. One of the major connectivity differences in these parts is

the Analog Mux Bus or AMux. The AMux gives connectivity to all GPIOs instead of eight pins on Port0 and four pins on Port2. Notice in Table 1 that all PSoC parts that have an AMux bus have more than twelve analog inputs. For specific information on these PSoC families, see the device datasheet and the **Analog System** section of the Technical Reference Manual (TRM) for that specific part family.

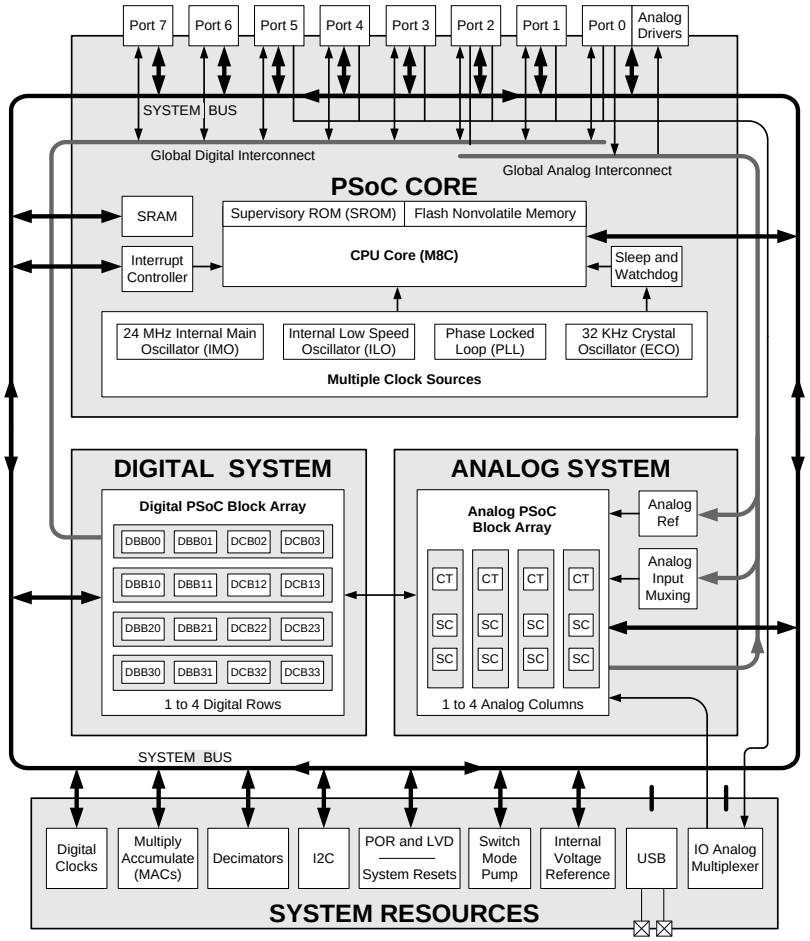
Table 1. Device Families Covered in this Application Note

PSoC Part Family	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	Limited Analog Blocks	Analog Mux Bus (AMux)
CY8C29x66	12	4	4	12	0	No
CY8C27x43	12	4	4	12	0	No
CY8C24x94	48	2	2	6	0	Yes
CY8C24x23	12	2	2	6	0	No
CY7C64215	48	2	2	6	0	Yes
CY8C28x23	10	2	2	6	0	No
CY8C28x33	40	2	4	6	4	Yes
CY8C28x43	44	4	4	12	0	Yes
CY8C28x45	44	4	4	12	4	Yes
CY8C28x52	24	4	4	12	4	Yes

PSoC 1 Architecture

PSoC 1 devices are divided into four sections, analog system, digital system, PSoC core, and system resources. Each of these sections vary in size and complexity depending on the part family. Figure 1 shows a block diagram of the standard PSoC 1 device.

Figure 1. PSoC 1 Block Diagram



The analog PSoC block array is the focus of this application note. It consists of two basic analog blocks known as continuous time (CT) and switch capacitor (SC). Due to the configuration flexibility of these blocks, all the analog user modules, such as ADCs, DACs, and PGAs, available in PSoC Designer are created using these two basic blocks. The analog user modules created with these blocks include several ADCs, DACs, filters, mixers, PGAs, and other components.

The Digital PSoC Block Array can contain between 4 to 16 blocks, depending on the device family. These digital blocks are used for components such as Counters, Timers, PWMs, UARTs, and SPI. They are also used in conjunction with analog blocks to create the timers and counters required in an ADC user module. This application note does not cover the digital blocks other than connectivity between the analog and digital blocks.

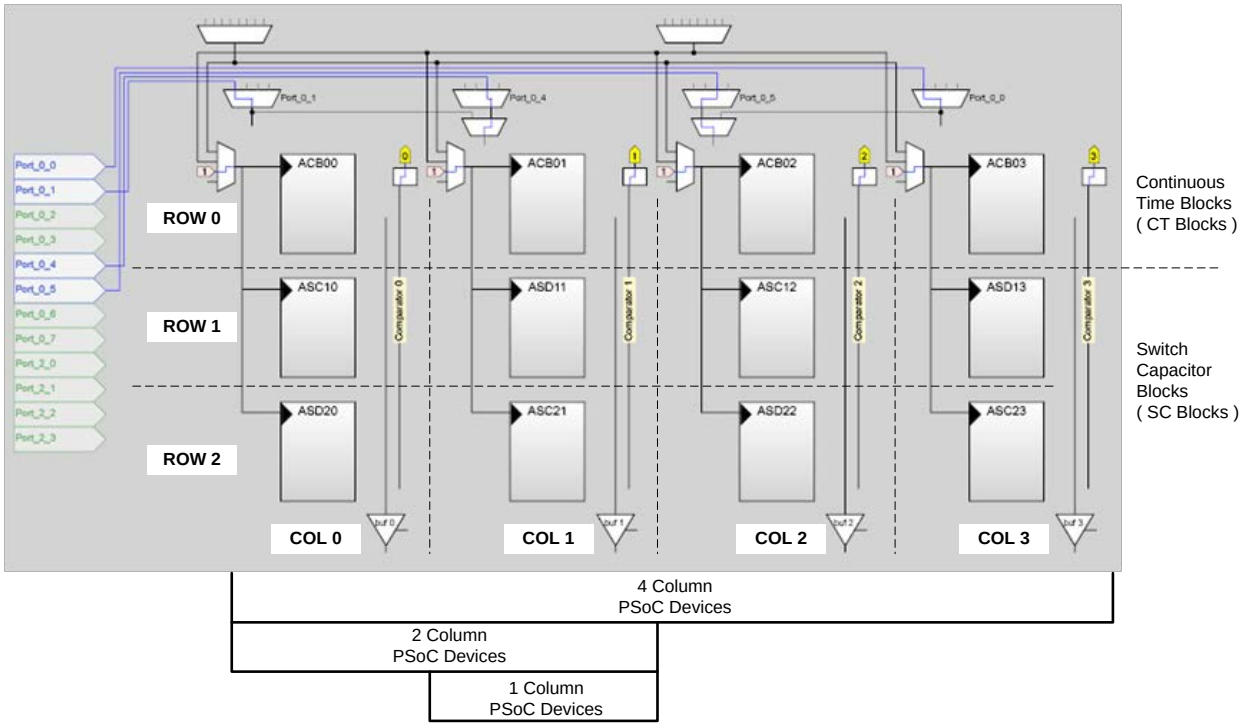
The system resources section can include fixed function blocks, such as I^2C, switch mode pump, USB, internal voltage reference, and I/O analog multiplexer. The actual resources available are dependent on the part family.

The PSoC core contains the CPU, SRAM, flash ROM, interrupt controller, oscillators, and GPIOs. As with the other blocks, different parts will have a variation of ROM and RAM sizes. Different packages will also limit the total number of GPIOs. The connectivity between the analog section and the GPIO pins are described in the application note.

Analog PSoC Block Array

When you open PSoC Designer and create a new project using one of the PSoC 1 parts such as the CY8C29x43, the **Chip** view displays two groups of blocks. The upper section shows the digital blocks and the lower section shows the analog blocks. Figure 2 shows an example of the analog block section. Other device families show a similar view but with a different number of available blocks and interconnection between blocks and GPIO pins. The row and column identifiers have been added to help clarify the block location later in the document.

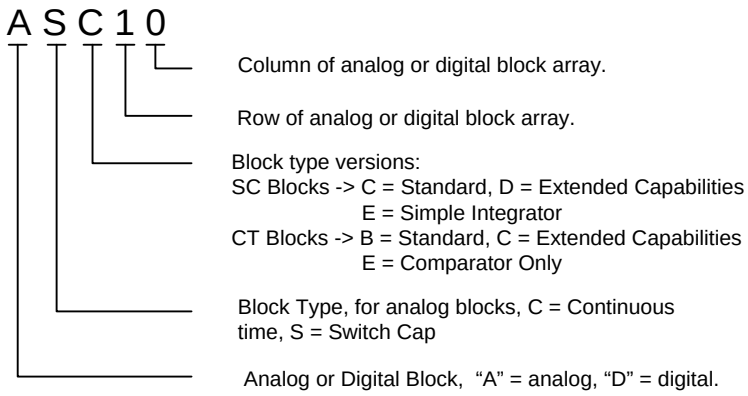
Figure 2. Analog Block Orientation for the CY8C29x44



The analog section is composed of one or more analog columns depending on the exact device you have selected. The CY8C29x44 contains four columns of analog blocks. Devices with a single column use column 1 and two-column devices use columns 0 and 1. The CY28xxx devices have four columns similar to the CY8C29x44 shown in Figure 2, plus two additional columns with limited analog functionality, mainly for use with CapSense. Table 1 summarizes the analog block and analog column count for each part type discussed in this application note.

Each block is labeled with a block identifier that shows the location and block type. An example of the format is ASC10. The “A” means that it is an analog block. The “S” identifies this as a switched capacitor block type. The “C” determines the type of switch cap block. Location of the block in the analog matrix is determined by the last two digits. In this example, the “10” determines that this block is located in row 1 and analog column 0.

Figure 3. Block Decoder

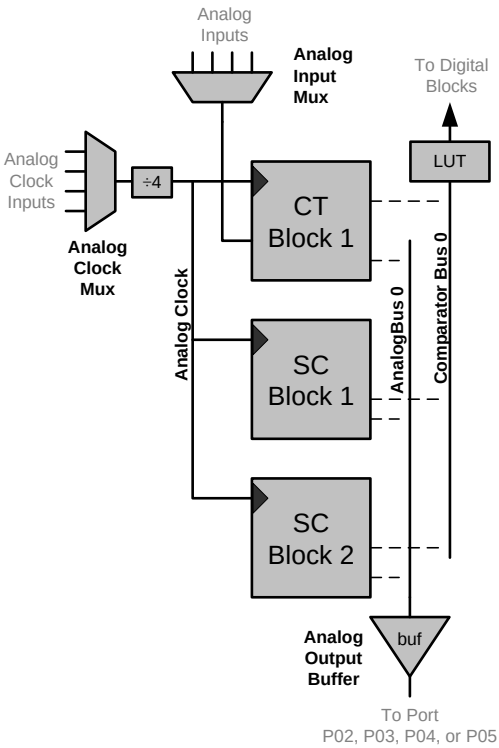


Analog Column Structure

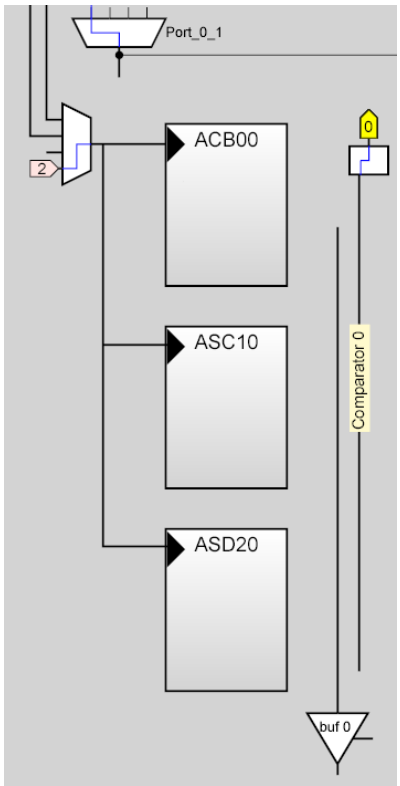
The standard PSoC 1 analog column consists of one CT block, two SC blocks, analog input mux (multiplexer), analog bus, comparator bus, analog output buffer, and an analog clock mux. See Figure 4 for more details. Each part of the analog column structure is discussed in the following sections.

Figure 4. Analog Column Structure

Chip View



PSoC Designer View

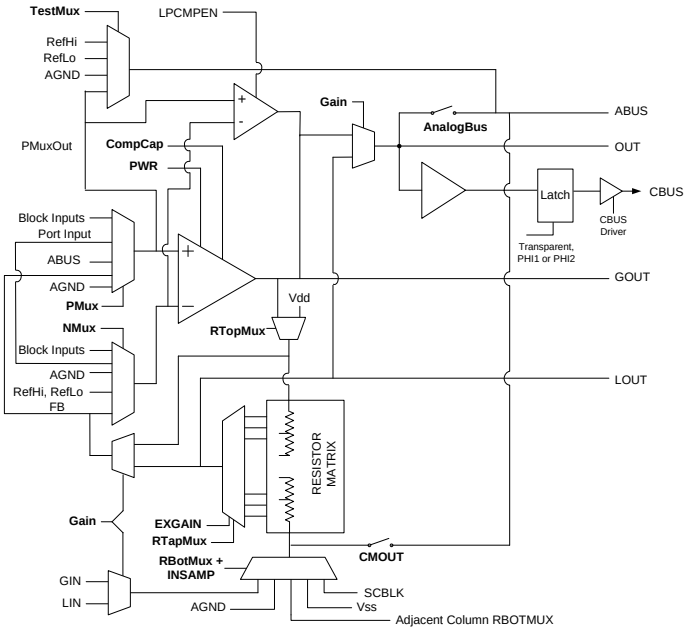


CT Blocks

The core of a CT block is a basic op-amp. Other components such as a resistor string, several analog muxes, and a comparator output are included to add flexibility. You can configure this block in a number of different ways to create several PSoC Designer user modules. Figure 5 shows the basic structure of a CT block. Following are some of the user modules in the PSoC Designer library that are constructed with an analog CT block:

- Inverting Amplifier (AMPINV)
- Comparator (COMP)
- Instrumentation Amplifier (INSAMP)
- Programmable Gain Amplifier (PGA)

Figure 5. PSoC CT Block



SC Blocks

The other two blocks in the analog column are Switch Capacitor or SC blocks. The SC blocks are flexible and used for a wide range of user modules. The most common use is a modulator, which is used for the PSoC ADCs (analog to digital converter). Here are the current user modules that use the PSoC 1 SC blocks:

- All PSoC 1 incremental and DelSig ADCs (such as ADCINC, ADCINCVR, DelSigPlus, DUALADC, and TRIADC)
- All PSoC 1 DACs (DAC6, DAC8, DAC9, MDAC6, and MDAC8)
- Analog filters (LPF2, LPF4, BFP2, BFP4, ELPF2, and ELPF4)
- DTMF dialer
- Generic SCBLOCK

Figure 6 and Figure 7 are the two basic SC blocks that are placed in the analog block matrix, in an alternating fashion. For more information about SC blocks, see AN2041 - Understanding PSoC 1 Switch Capacitor Analog Blocks. To learn more about implementing switch cap filters in PSoC 1, see AN2168 - PSoC 1 Understanding Switched Capacitor Filters.

Figure 6. PSoC 1 SC Type C Block

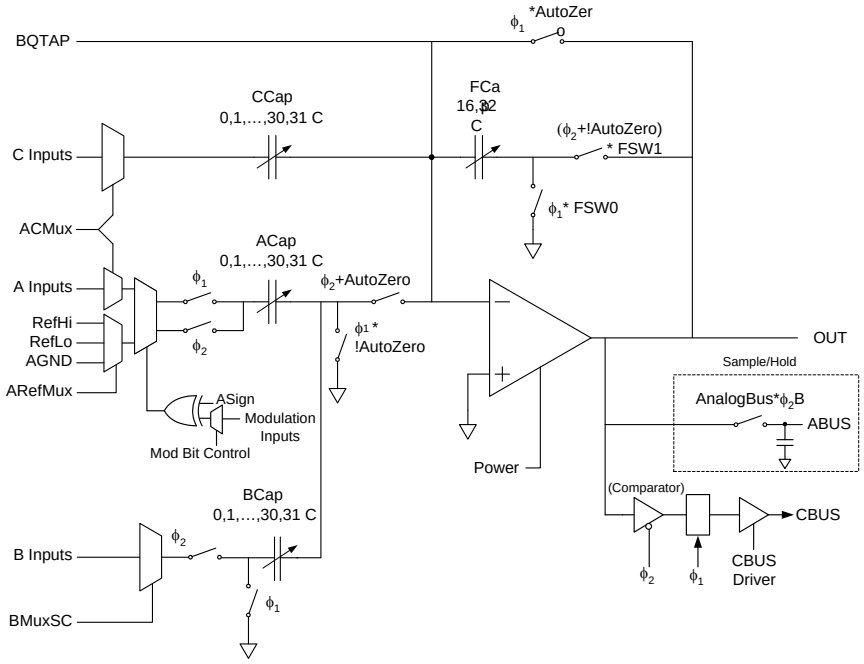
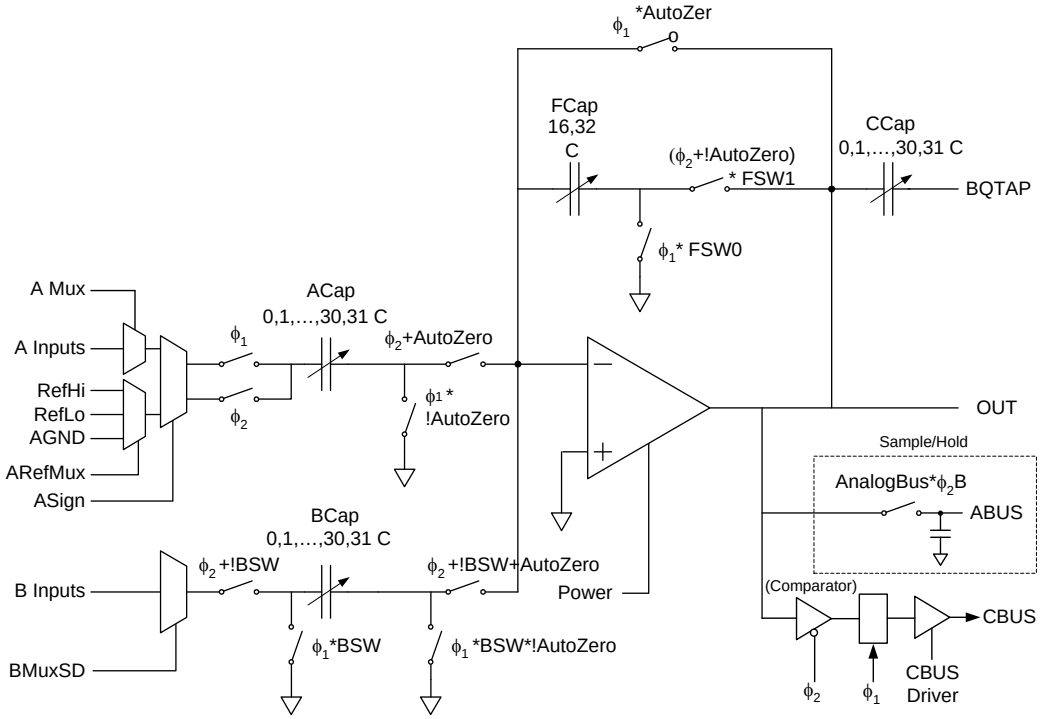


Figure 7. PSoC 1 SC Type D Block



Analog (Column) Bus

The analog bus is primarily used to route an analog signal from one of the analog blocks to the analog output buffer (for more information, see the Analog Output Amplifier section). Any user module that outputs an analog signal such as an amplifier, DAC, or filter can drive the analog column bus. PSoC Designer allows one analog block to drive the analog bus, but it is possible to set registers during runtime that enable more than one block to drive the bus at the same time. Be sure to disconnect the previous block before the second is connected, to avoid shorting two outputs.

Analog user modules that have an input and are placed in the SC block at the bottom of the column (Row 2), may use the analog bus as an input source. This way, the analog column bus can be used to route a signal from a CT block (row 0) output to the input of an analog user module located on the bottom (row 2) of the analog column.

Analog Output Amplifier

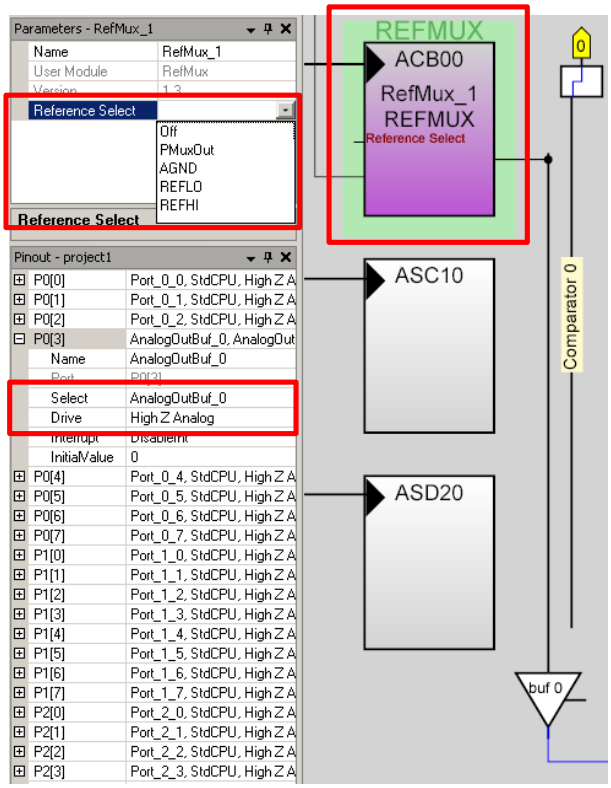
Each column has an analog buffer that is connected to the analog column bus. If enabled, this buffer can drive 30 to 40 mA depending on the device family. Each buffer is connected to a dedicated GPIO pin. The four columns, 0 through 3, are connected to pins P02, P03, P04, and P05, respectively. If the buffer is enabled, the signal on the analog bus will be buffered and driven to the associated pin. If the buffer is disabled, the pin will operate as a standard GPIO pin. The buffer may also be bypassed and the non-buffered signal driven directly to the pin, but this is not recommended because of the low drive strength of the analog blocks.

Any analog block output that needs to be routed to an external GPIO pin should be buffered by the analog buffer to provide sufficient signal strength. Common uses for the analog buffer include:

- DAC output buffer
- Analog ground buffer (virtual ground)
- Filter output
- Reference signal output (RefHi, RefLo, and AGND)
- Buffer external signal (in one pin, through the buffer, then out another pin)

To buffer an internal reference, the **RefMux** User Module may be placed at the top of the column (row 0) in the CT block location. The **Reference Select** parameter of the RefMux User Module is used to select one of the three analog reference voltages (AGND, REFLO, or REFHI) or an input from the GPIO pins through the PMux (Positive Input Mux). Figure 8 shows the RefMux parameter selection and the configuration of P0[3], which is the output of the analog buffer for column 0. Note that the GPIO **Drive** mode is set to **High Z Analog** and the **Select** parameter is set to the buffer **AnalogOutBuf_0**.

Figure 8. Setting Up RefMux User Module

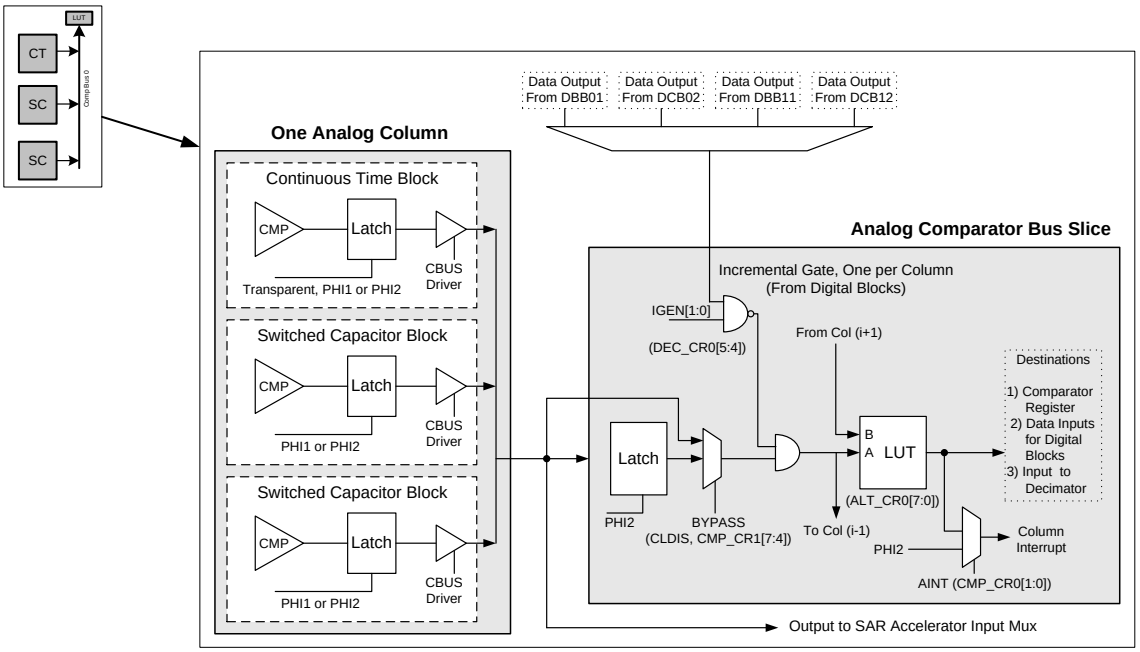


Comparator Bus

Each analog column has a dedicated comparator bus associated with it. Every analog PSoC block has a comparator output that can drive this bus. However, only one analog block in a column can actively drive the comparator bus at a time. The comparator bus output may be routed to a digital block as a signal source. It also serves as an input to the decimator (used for ADCs), serves as an interrupt input, and is available as read-only data in the Analog Comparator Control register (**CMP_CR0**).

In the CY8C28xxx families, the comparator signals may also drive several of the digital signal buses to give even more flexibility to digital block inputs and directly driving pin outputs.

Figure 9. Comparator Bus and Interface



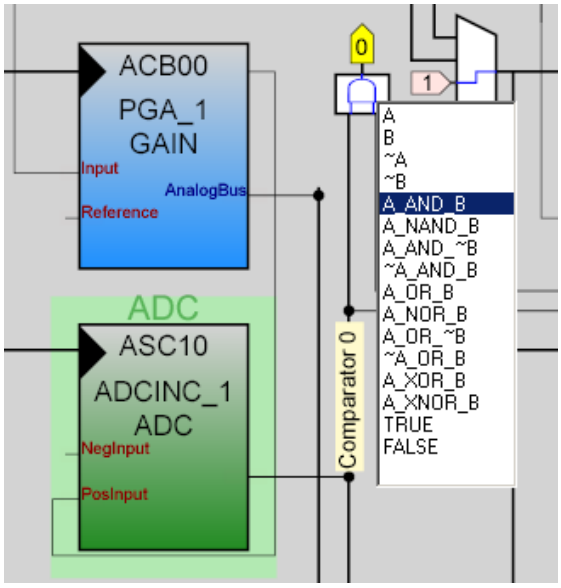
The Comparator Buses contains a digital look-up table (LUT). This LUT includes several logic functions that can combine the signal of the comparator bus with that of the comparator bus to the right. Table 2 shows the possible combinations for the LUT. **A** is the signal from the current comparator bus and **B** is the signal from the comparator in the column to the right. If you are configuring the right most column LUT, the **B** input is from the left most column. When reading register **CMP_CR0** to check the status of the comparator, this is the **output of the LUT**, which may not be the actual Comparator Bus state, depending on the LUT option selected.

Table 2. Comparator Look-up Table (LUT) Options

Logic Function	Description
A	Column Comp Bus
B	Adjacent Comp Bus
~A	Inverted Column Comp Bus
~B	Inverted Adjacent Comp Bus
A AND B	Logical AND of A and B
A AND ~B	Logical AND of A and not B
~A AND B	Logical AND of not A and B
A OR B	Logical OR of A and B
A NOR B	Logical NOR or A and B
A OR ~B	Logical OR of A and not B
~A OR B	Logical OR of not A and B
A XOR B	Logical XOR of A and B
A NOR B	Logical NOT of A and B
TRUE	Output always high
FALSE	Output always low

If you click on the LUT in the PSoC Designer interface, as shown in Figure 10, you can see the available logic options. A logic symbol appears in the LUT box after a function is selected. Notice in Figure 10 that an AND gate is shown. Because there is only one comparator bus per analog column, only one user module that requires a comparator output can be placed in a single column. If a design has more than one user module that requires the comparator bus, be sure to place each of them in separate analog columns. Most ADCs such as the Delta-Sigma make use of the comparator output to interface to a counter or decimator. The comparator (COMP) and Generic SCBlock components are two other user modules that use the comparator bus.

Figure 10. Selecting Comparator Bus LUT Option

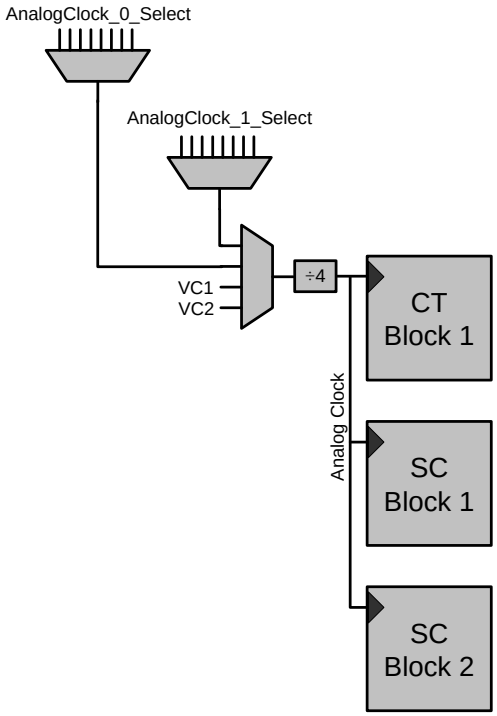


Analog Clock

The SC blocks require a two-phase, non-overlapping clock to drive the SC block internal switches. This two-phase clock is derived from the clock connected to the analog column. The CT blocks use this clock when in the comparator mode to sync the output to the SC blocks and any digital blocks that it may be connected. A separate analog column clock generator is provided for each column. It is important to note that **regardless of the clock source selected, the output frequency of the column clock generator is the input frequency divided by four in the column.** This is done to generate the non-overlapping clocks.

Figure 11 shows the analog clock tree for an analog column. Each of the AnalogClock_x_Select muxes selects one of the digital blocks for the clock source. The global clocks, VC1 and VC2, may also be selected as the clock source.

Figure 11. Analog Clock Tree



When analog signals are routed between blocks in adjacent columns, the clocks in these columns should be synchronized in phase and frequency. Frequency synchronization may be achieved by selecting the same input clock source for the columns.

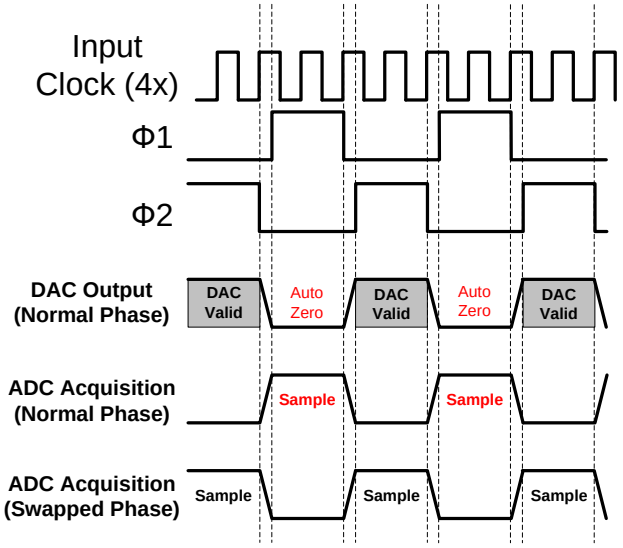
Most components based on the switch cap blocks have a **ClockPhase** option. Phase synchronization is accomplished using this option. In some cases careful thought must be given to verify a long signal chain is properly synchronized.

The selection of the Clock Phase is used to synchronize the output of one switched capacitor analog PSoC block to the input of another. The switched cap analog PSoC blocks use the two-phase clock (φ1, φ2) to acquire and transfer a signal. Typically, the input to an ADC is sampled when φ1 is high, the Normal setting. A problem arises in that many of the user modules auto-zero their output during φ1 and provide a valid output only during φ2. If such a module's output is fed to the ADC's input, the ADC acquires an auto-zeroed output instead of a valid signal. The clock phase selection allows the phases to be swapped so the input signal is now acquired during φ2, the "Swapped" setting.

Figure 12 illustrates an example were a voltage DAC output is only valid during φ1, but by default the ADC is sampled during φ2. This causes the ADC to read the DAC's output during its auto zero cycle instead of when

the output is valid. By changing the clock phase option of the ADC to “Swapped” you can see the ADC sampling at the correct time. Each user module will identify the phase that it acquires or outputs its signal in the **ClockPhase** parameter section of the datasheet.

Figure 12. Normal and Swapped Clocks



Looking at the “DAC Output” waveform in Figure 12, you may become concerned that the DAC output does not look like a continuous signal. Internally an SC block output will switch between its auto-zero and valid phase, but as long as the SC blocks are synced properly, this is not a problem. When routing the signal to the analog column bus, it passed through a sample and hold circuit. Each analog column has its own sample and hold, which convert the SC block output back to a continuous time signal.

The sample and hold circuit consists of a switch controlled by φ2, an internal capacitor, and an op-amp configured as a voltage follower. The voltage follower is the analog buffer at the bottom of the analog column. The sample and hold capacitor is charged while φ2 is high and is held when φ2 is low. See Figure 13 for more details.

Figure 13. Analog Column Sample and Hold Circuit

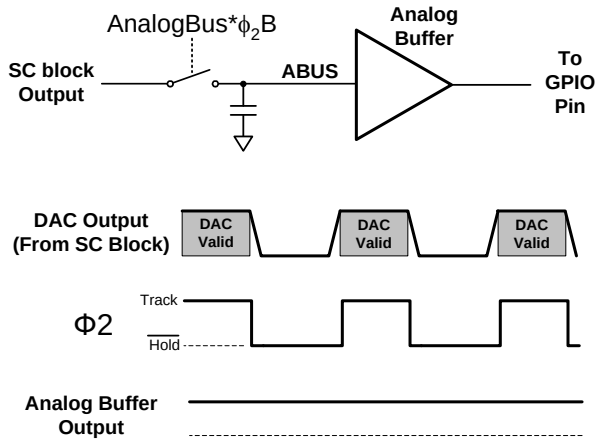


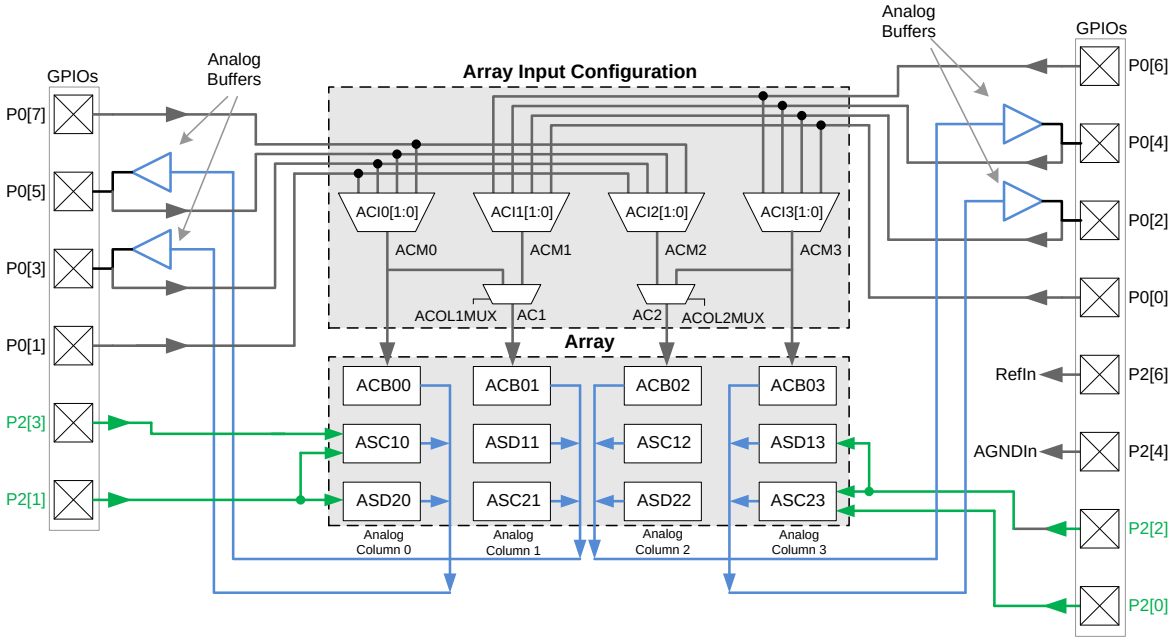
Figure 6 and Figure 7 of the SC blocks show the sample and hold capacitor in the block for simplicity, but it is actually a part of the analog column.

Analog Connectivity to GPIO Pins

Connectivity between the analog column inputs and the GPIO pins varies between PSoC 1 families, but all devices discussed in this application note have the standard Port0 and Port2 connectivity. Port0 pin signals can be routed directly to the columns. The odd Port0 pins are connected directly to columns 0 and 2 (the even columns), and even Port0 pins are connected to columns 1 and 3 (the odd columns). Columns 1 and 2 have an additional mux that allow these columns to access all pins on Port0. See Figure 14 for a representation of the basic connectivity.

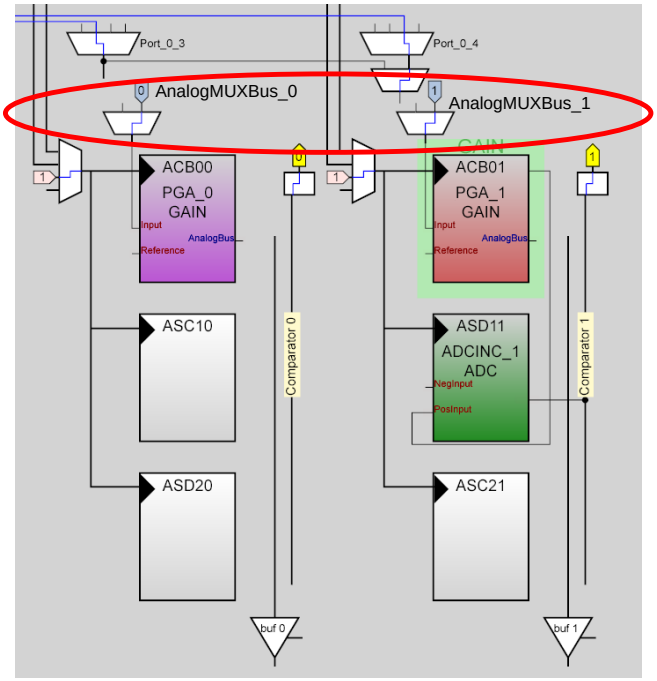
Figure 14 also shows a few more connections to the SC blocks in columns 0 and 3 from Port2 (Note the routes in green). The additional connections allow direct GPIO connectivity to these analog SC blocks and add four more analog inputs to components such as ADCs, mixers, and filters. The routes in blue are the analog column buses that any one of the three analog blocks can drive. The signal on the analog bus can then drive a dedicated GPIO pin with the Analog Output Amplifier.

Figure 14. Basic Analog Connectivity



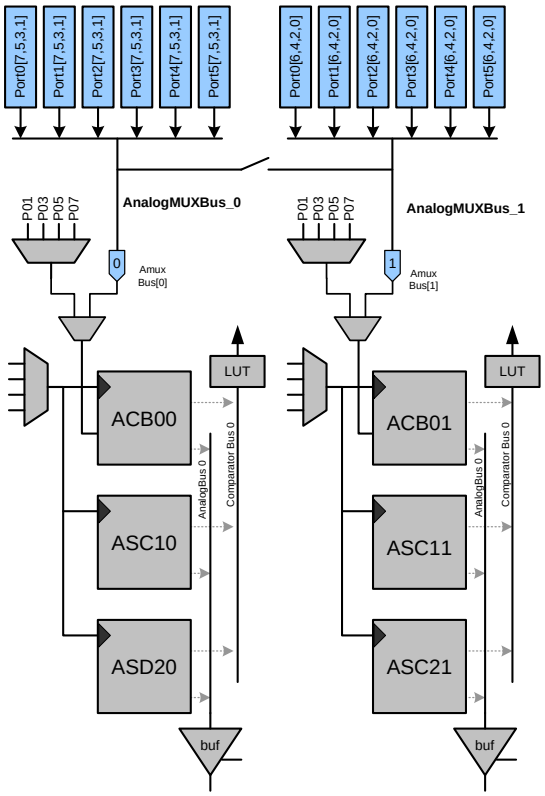
There are several variations to this interconnectivity diagram depending on the device family. The biggest differences as mentioned previously are the number of columns and the addition of the AMux bus that allows all the GPIOs to be configured as analog inputs. In the chip diagram in PSoC Designer, a third layer of analog muxes is added to parts that contain the AMux bus. The extra layer provides connectivity between the analog columns and all of the GPIOs pins, not just Port0 and a few pins of Port2. Figure 15 shows an example with one of the CY8C24xxx devices.

Figure 15. Example of CY8C24x8x AnalogMUXBus connections shown in PSoC Designer



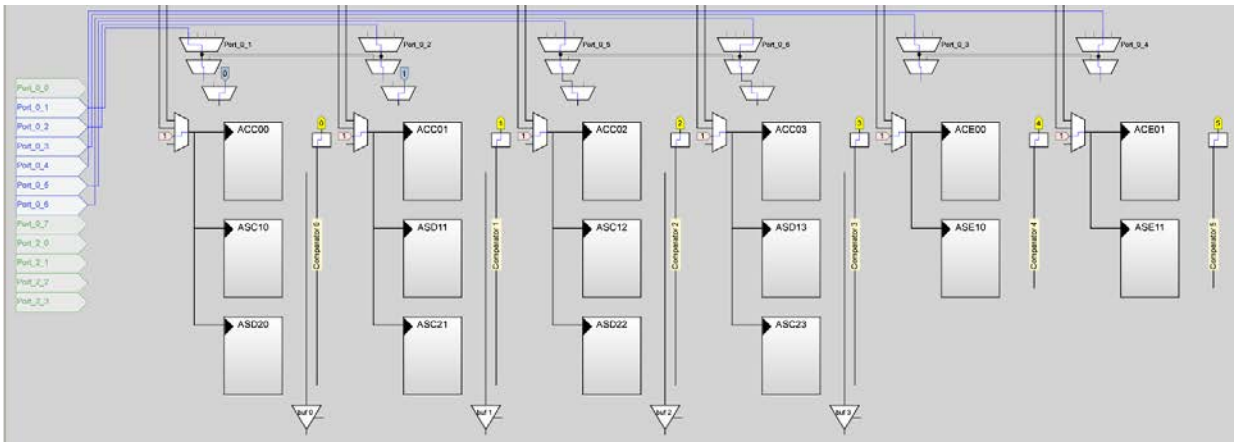
The CY8C24x8x parts have two AnalogMUXBuses that may be used independently or combined together. The Odd port pins may connect to AnalogMUXBus_0 and the even pins can be connected to AnalogMUXBus_1. These buses may be used to route any analog signal to one of the analog columns, or be used for CapSense in the parts that support it. Figure 16 shows port pins that can connect to each of the buses.

Figure 16. AnalogMUXBus Conectivity



The CY8C28xxx devices have a similar architecture but extend it to four full analog columns. Two additional columns shown on the right side in Figure 17 have limited functionality. These two additional columns have a CT block of type ACE and a switch cap block of type ASE. The CT blocks (Type ACE) are built around a low-power, low-offset amplifier. They can be configured in two modes: as a unity gain buffer to drive the other column or open loop as a comparator. The ASE blocks are special hardware used in conjunction with the ACE blocks for CapSense.

Figure 17. CY8C28xxx Example Analog Structure



You may configure initial analog routes in PSoC Designer during design. They will be configured prior to user code execution (*main.c*). For applications in which some or all analog routes don't need to change during runtime, you do not need to generate additional code.

If the input to a specific user module has to change during runtime, you can either write code to configure the mux registers directly or take advantage of the analog mux user modules provided. Table 3 provides a list of analog mux user modules available for each family.

Table 3. Available Mux User Modules

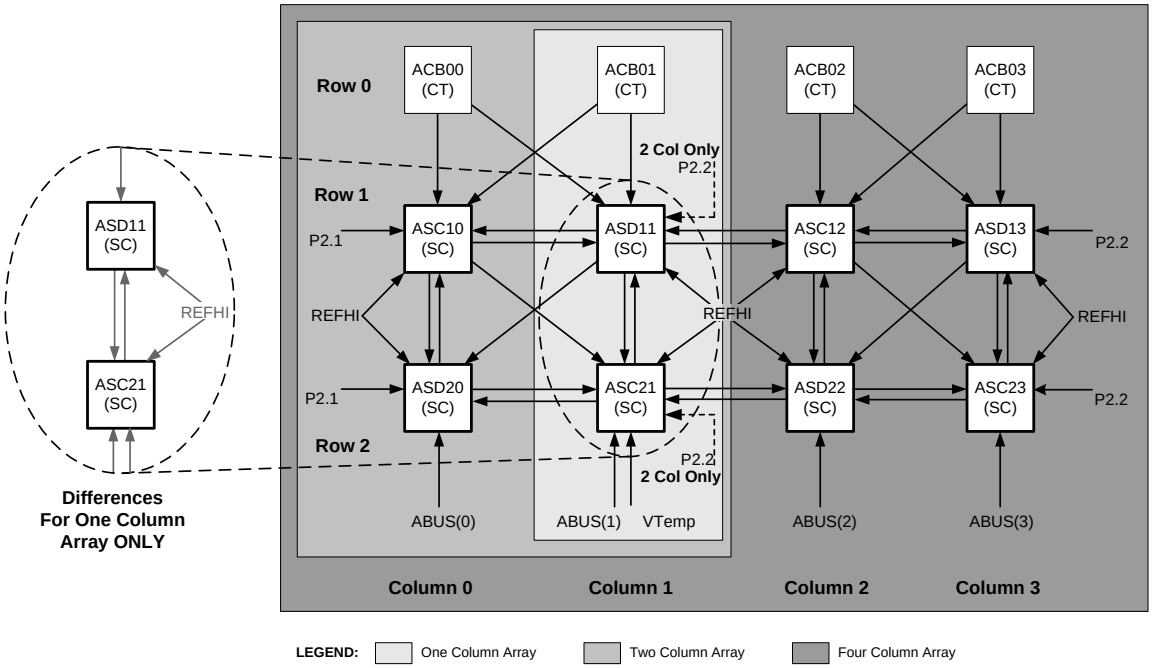
PSoC Part Family	Analog Inputs	Analog Mux Bus	Analog MUX User Modules	Description
CY8C29x66 CY8C27x43 CY8C24x23	12	No	AMUX4 AMUX8	Port0, 4 input mux Port0, 8 input mux
CY8C24x94	48	Yes	AMUX4 AMUX8	Port0, 4 input mux Port0, 8 input mux
CY7C64215	48	Yes	AMUX4 AMUX8 AMuxN	Port0, 4 input mux Port0, 8 input mux All GPIO pins
CY8C28x23	10	No	AMUX4 AMUX8	Port0, 4 input mux Port0, 8 input mux
CY8C28x33	40	Yes	AMUX4 AMUX8 AMuxN	Port0, 4 input mux Port0, 8 input mux All GPIO pins
CY8C28x43 CY8C28x45	44	Yes	AMUX4 AMUX8 AMuxN	Port0, 4 input mux Port0, 8 input mux All GPIO pins
CY8C28x52	24	Yes	AMUX4 AMUX8 AMuxN	Port0, 4 input mux Port0, 8 input mux All GPIO pins

Internal Analog Block Interconnect

Other than connectivity from the input muxes and the analog column bus, each analog block may connect to most nearby analog blocks. Figure 18 shows an example of the connectivity available. These routes are independent of the input routing from Port0, the analog column bus, and AMux bus. The inputs from Port2 are also shown in the diagram to show all the direct inputs to the analog blocks.

Each PSoC 1 family has different connectivity options, but the concepts are similar. It is important to review the Analog Section of the Technical Reference Manual (TRM) for the part you have selected, to ensure you understand the options that benefit your design.

Figure 18. Inter-Analog Block Connectivity



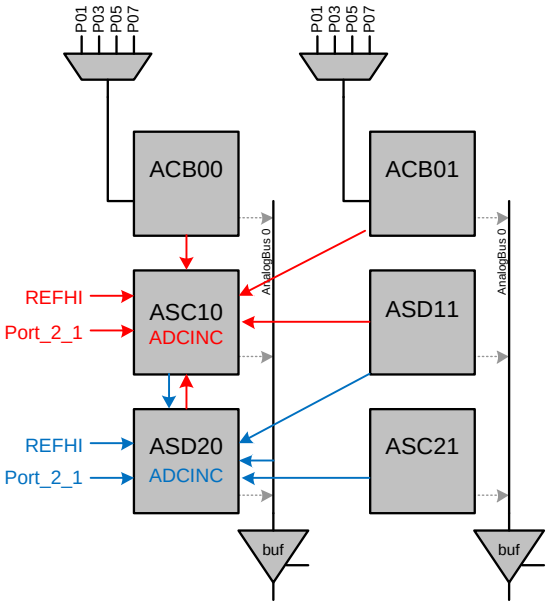
PSoC Designer understands these routes and adjusts the input and output parameters when a user module block is moved from block to block.

See Figure 19 for an example where input options are dependent on the user module block placement. If the analog block for an ADCINC user module is placed in row 1 of the first column, the connection options are different compared to when the block is placed in row 2. The red and blue arrows illustrate the possible positive input options for the ADCINC. Table 4 shows the possible options for the ADCINC positive input for each of the blocks ASC10 and ASC20. Note that most of the connections are different.

Table 4. ADCINC Input Options

ADC placed at ASC10 (row 1)	ADC placed at ASD20 (row 3)
ACB00	ASC10
ASD11	Port_2_1
REFHI	ASC21
ASD20	AnalogOutBus_0
ACB01	REFHI
Port_2_1	ASD11

Figure 19. Example Input Options for ADCINC



Internal Reference Structure

The PSoC Programmable System-on-Chip operates on a single power supply between 3.0 and 5.25 V. Analog signals in most systems are typically of both positive and negative polarity around a reference usually ground. The PSoC only handles signals of positive polarity with respect to V_{SS} chip ground. A virtual analog ground (AGND) is generated on the chip to provide a reference point for signals that swing both positive and negative relative to AGND. This virtual ground needs to be between V_{SS} and V_{DD}, and far enough from each supply rail so the signals relative to it will not be clipped by the supply. PSoC 1 parts have several internally generated options and an option to use an externally generated signal as a virtual ground reference.

Three reference voltages dictate the range of the DACs, ADCs, and other analog components. These references, AGND (Analog Ground), RefHi (Reference High), and RefLo (Reference Low) are generated based on either an internal bandgap reference, supply voltages (V_{SS} and V_{DD}), or external reference voltage.

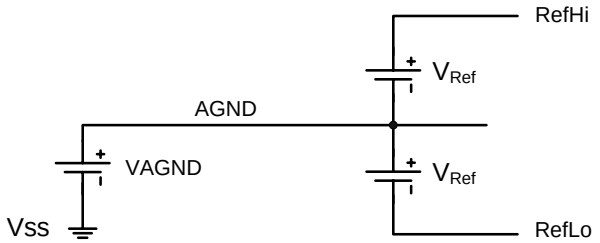
An internal bandgap reference generates a stable 1.3 V V_{REF}. This reference is referred to as the BandGap. Several of the reference options use the BandGap reference to generate the AGND, RefHi, and RefLo signals. The relationship between these signals is as follows; RefLo < AGND < RefHi. The equations are used to calculate RefHi and RefLo based on AGND and V_{REF}. V_{REF} is derived from the BandGap, V_{DD} (chip power), or an external reference signal.

$$RefHi = AGND + Vref$$

$$RefLo = AGND - Vref$$

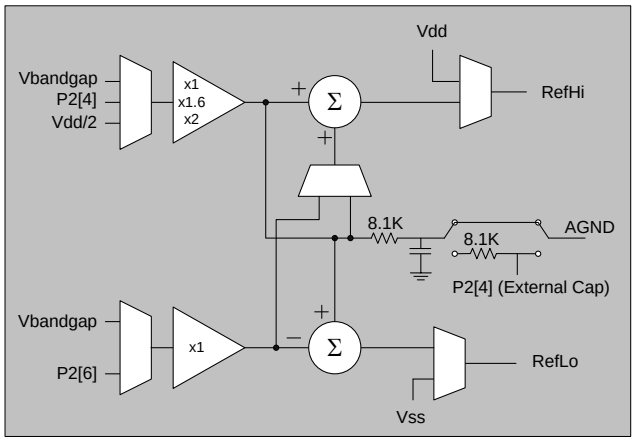
The RefLo and RefHi signals are important because they define the upper and lower range of the DACs and ADCs. V_{REF} can be the internal BandGap voltage (1.3 V) times a constant, $V_{DD}/2$, or an external signal connected to pin P2[6]. Analog Ground (AGND) may be generated by $V_{DD}/2$, derived from the BandGap, or from an external source connected to pin P2[4]. A simplistic view of the AGND, RefHi, and RefLo signals is shown in Figure 20.

Figure 20. Simplistic View of RefHi, RefLo, and AGND



A simplified schematic of the reference (AGND, RefHi, RefLo) generation circuit is shown Figure 21.

Figure 21. Block Diagram of Reference System



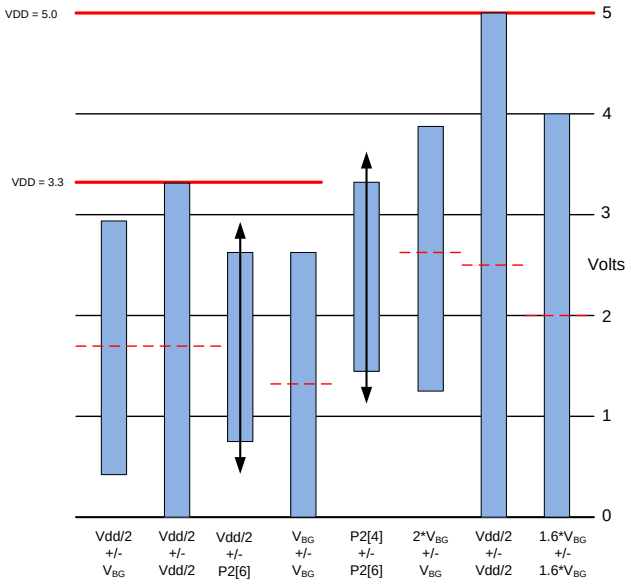
If you use the RefHi and RefLo equations and understand the simple reference schematic, you can calculate the reference voltages for each of the settings. Table 5 shows each of the calculated reference voltages. Note that not all options are useful for all supply voltages, because RefLo and RefHi should always be within the V_{SS}-to-V_{DD} range. For measurements that are referenced to V_{SS}, the options where RefLo is equal to V_{SS} will be the best choice. It is good design practice to ensure that the signal being measured uses either RefHi, RefLo, or AGND for its reference.

Table 5. Calculated AGND, RefHi, and RefLo

Ref Mux Option	Vdd	RefLo	AGND	RefHi
(V_{DD}/2)+/- BandGap	3.3 V	0.350 V	1.65 V	2.95 V
	5.0 V	1.2 V	2.5 V	3.7 V
(Vdd/2)+/-(Vdd/2)	3.3 V	0.0 V (V_{SS})	1.65 V	3.3 V (V_{DD})
	5.0 V	0.0 V (V_{SS})	2.5 V	5.0 V (V_{DD})
BandGap +/- BandGap	3.0 V to 5.0 V	0.0 V (V_{SS})	1.30 V	2.60 V
(1.6*BandGap)+/- (1.6*BandGap)	> 4.16 V	0.0 V (V_{SS})	2.08 V	4.16 V
(2*BandGap) +/- BandGap	> 3.9 V	1.3 V	2.6 V	3.9 V
(2*BandGap) +/- P2[6]	3.0 V to 5.0 V	2.6V – P2[6]	2.6 V	2.6 V + P2[6]
P2[4] +/- BandGap	3.0 V to 5.0 V	P2[4] – 1.3 V	P2[4]	P2[4] + 1.3 V
P2[4] +/- P2[6]	3.0 V to 5.0 V	P2[4] – P2[6]	P2[4]	P2[4] + P2[6]

Figure 22 is a graphical representation of Table 5 to help illustrate the useful input and output range of SC-based user modules, for supplies of 3.3 V and 5.0 V.

Figure 22. Reference, DAC, and ADC Ranges



The op-amps in the reference outputs require a certain amount of headroom, typically 0.3 V from each supply rail. When the analog ground and reference are derived from external sources, the RefHI and RefLO signals should meet this requirement.

In cases where the reference is the supply rail (for example, V_{DD}/2 +/- V_{DD} /2, RefHI = V_{DD}, RefLO = V_{SS}), the reference output op-amps are switched off and the reference is simply switched directly to the appropriate supply rail.

DAC outputs are scaled to the reference values (RefHi and RefLo), see Figure 22. Ensure that DAC outputs connected to external loads, use the analog output buffers. The SC blocks are designed to drive only other internal analog blocks.

The analog output buffers in the PSoC are not rail-to-rail, but typically reach 0.4 V from V_{SS} and 0.6 V from V_{DD}, at rated load, so system designs should accommodate this output swing even if the reference outputs are set to V_{DD} or V_{SS}. Refer to the device datasheet for the rated load of the analog buffer.

Table 6 provides a summary of each reference option and suggests the selection that can work best for an application.

Table 6. Ground and Reference Selections

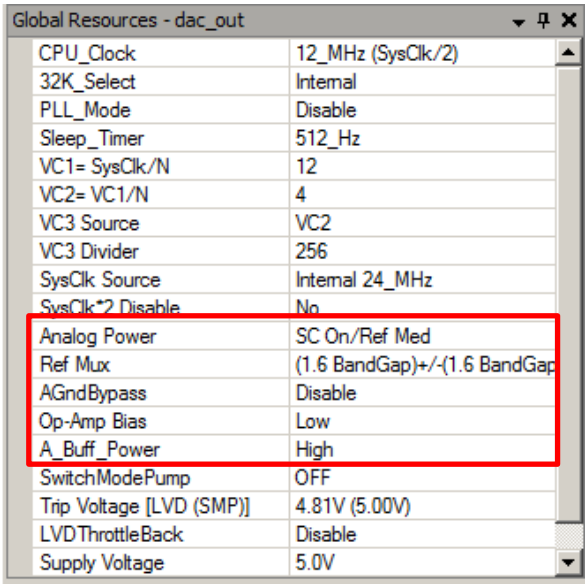
Selection	Application
V_{DD}/2 +/- BandGap	Systems using differential sensors or AC coupled measurements where absolute voltages are measured. A good example is audio signal processing.
V_{DD} /2 +/- V_{DD} /2	Systems using sensors with outputs that are ratiometric to the power supply voltage and need analog-to-digital converters with input range tracking the supply voltage. V_{DD} connected pressure sensors are a good example.
BandGap +/- BandGap	Systems requiring measurements that are absolute (that is not ratiometric to the supply) effectively use this selection. Examples include battery measurement or system power supply monitoring.
1.6*BandGap +/- 1.6*BandGap	This setting is used by systems requiring absolute measurements with wider range than 2*BandGap full scale. Note that 4.16 volts is very close to 1 mV per bit for 12-bit systems.
2*BandGap +/- BandGap	Used for systems with limited range centered at a fixed voltage. Commonly used for resistance and thermistor temperature measurements as in AN2017.
2*BandGap +/- P2[6]	Used for systems with absolute measurements with user-specific ADC input range, typically with higher sensitivity around the nominal analog ground. The limit in this case is the build-up of offset voltages in the reference generation; this limits the minimum value of user-supplied reference to greater than 0.5 V.
P2[4] +/- BandGap	Used for systems with absolute measurements with a user-specific analog ground value. This is typical of systems where the sensor also outputs a specific reference near mid-supply and this level is an essential part of system calibration.
P2[4] +/- P2[6]	Used for systems where the user supplies external values for both ground and reference. Typically, this is for systems where the analog ground is set at a specific offset and the user needs a limited range for ADC inputs with higher resolution. The resolution limit is set by the offset error contribution in the reference generator.

Global Analog Parameters

PSoC Designer has several global settings that affect the entire design, including most of the analog user modules such as ADCs, DACs, filters, and amplifiers. These global settings appear in the PSoC Designer window. The analog parameters of interest are circled in red shown in Figure 23 and listed as follows.

- Analog Power
- Ref Mux
- AGndBypass
- Op-Amp Bias
- A_Buf_Power

Figure 23. PSoC Designer Global Resources



The analog global parameter settings are a way to set the initial conditions for PSoC analog parameters. Most of these settings are set once during power-up, and never changed, however some applications may need these parameters to be changed during runtime. At that time, these parameters can be changed individually by register writes. The ARF_CR register controls the Analog Power,

Ref Mux, and Op-amp bias control. ABF_CR0 controls the analog output buffer power (A_Buff_Power). To enable the AGND Bypass mode, use the BDG_TR register. (The AGND Bypass is discussed later in this document.) Because most registers control more than one function, take care to modify only the bits for the function you want to modify. The TRM (Technical Reference Manual) for each PSoC 1 family gives a detailed description of each bit in the ABF_CR, ABF_CR0, and BDG_TR registers.

Analog Power

The analog power parameter sets the initial state of the analog SC, CT, and reference buffer power levels. It acts as a master switch to turn ON or OFF all analog blocks including the reference buffers. Each analog SC and CT block has its own power control that allows for four power settings: Off, Low, Medium, and High. All user modules that use at least one analog block include an API function that allows you to select the power level, such as “Start” and/or “SetPower”. The correct power level is dependent on the user module and the analog clock frequency used with the module. Table 7 is a valid list of settings for the analog Power parameter.

Table 7. Analog Power Settings

Analog Power Option	CT Block Power	SC Block Power	Ref Power
All Off	Off	Off	Off
SC Off / Ref Low	On	Off	Low
SC Off / Ref Med	On	Off	Med
SC Off / Ref High	On	Off	High
SC On / Ref Low	On	On	Low
SC On / Ref Med	On	On	Med
SC On / Ref High	On	On	High

For each of the two 'ON' cases, select reference drive levels of high, medium, and low to choose the current drive capability for the internal reference buffers. You need to select a good balance between performance and power consumption.

This selection affects the total power consumption of the PSoC. Each user module using the reference and the op-amp block associated with it adds slightly to the power consumed by the device. Because the internal reference is used as an integral part of most switched capacitor circuits, the current drive capability has an impact on the speed at which the switched capacitor block operates. In general, higher settings for this parameter allow switched capacitor circuits to operate at higher clock rates, at the expense of higher power consumption. To estimate the current (and power) consumption per op-amp block, see the applicable table in the datasheet for the part.

A_Buf_Power

The A_Buf_Power parameter allows you to select the power level for the analog output buffers that are connected to the analog column bus. These buffers are used to buffer internal analog signals that drive external pins on the PSoC. This power setting has little effect on the buffer frequency response but improves stability when driving capacitive loads. The “High” setting is recommended when the load capacitance is greater than 100 pF. When the load capacitance is 100 pF or less, it is best to use the “Low” setting to save power. Maximum load capacitance is about 200 pF.

AGndBypass

Some PSoC devices have the capability to provide an external analog ground (AGND) bypass capacitor to pin P2[4]. This reduces the switching noise to some extent that is present on the internal AGND. This feature is enabled by setting the **AGNDBypass** parameter to **Enable**. The GPIO pin P2[4] also has to be configured properly. The GPIO’s **Select** option should be set to **ExternalAGND** in the **Pinout** window as shown in Figure 24. Typical values for the external bypass capacitor are between 0.01 µF and 10 µF, and normally should not exceed 10 µF. The recommended value is 1 µF.

Figure 24. AGND Configuration

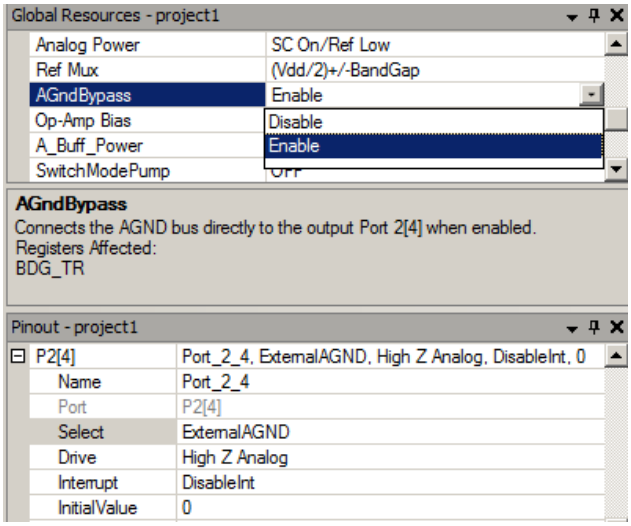
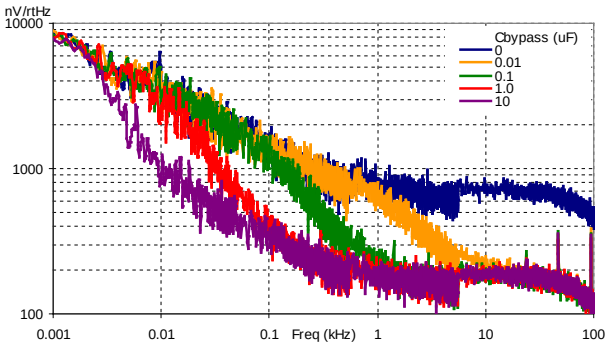


Figure 25 shows typical noise without a bypass capacitor and a range of capacitors between 0.01 µF and 10 µF. Note that as the capacitor value increases, the cutoff frequency decreases.

Figure 25. Typical AGND Noise with capacitor connected to P2[4], capacitor values in µF



Op-amp Bias

The Op-amp bias parameter adjusts the bias of all the op-amps in the continuous time and switch capacitor analog blocks. Performance of the internal op-amps is tailored based upon the application under development by selecting high or low bias conditions for the analog section of the PSoC. Selecting high bias causes the op-amp to consume more current but also increases its bandwidth and switching speed, lowering its output impedance. The total op-amp power consumption is a function of both the global “Op-Amp Bias” parameter and the individual power settings. To estimate the current (and power) consumption per op-amp block, including the effect from high or low selection of op-amp bias, refer to the applicable table in the datasheet for the part. To estimate the effect on AC op-amp parameters, refer to the applicable AC Operational Amplifier Specifications in the device datasheet. Table 8 shows minimum GBW for the analog block amplifiers with different power settings.

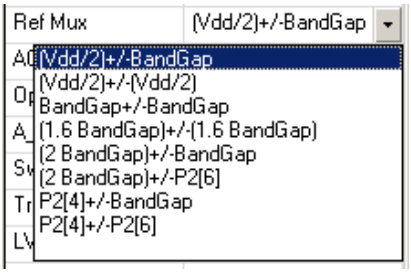
Table 8. Op-amp GBW with respect to Power and Bias settings

Individual Op-amp Power Setting	Op-amp Bias	Gain Bandwidth Product (Min)
Low	Low	0.75 MHz
Medium	High	3.1 MHz
High	High	5.4 MHz

Ref Mux

The Ref Mux parameter is probably the most important setting among the global analog settings as discussed previously. It determines the range and (potential) accuracy of any component that uses an analog SC block such as an ADC or DAC. Values specified with the Ref Mux parameter are in pairs and consist of [AGND level ± full scale]. See section Internal Reference Structure for more information. The reference chosen controls the maximum voltage that should be input to a switched capacitor circuit and output from a switched capacitor circuit. Both the analog ground (AGND) level and the peak-to-peak voltage are selected using this parameter. See Figure 26 for Ref Mux menu options.

Figure 26. Reference Selection Options



Analog voltage measurement and signal processing applications in PSoC 1 require the use of a precision ground and voltage references. Selecting the correct analog ground and voltage reference is essential in establishing accurate system performance. PSoC 1 offers considerable flexibility in setting references.

Trouble Shooting Incorrect ADC Operation

A number of configuration mistakes can cause the ADC to not work as intended or not work at all. Here is a list of these issues and how to fix them:

- **Clock Selection**: Most ADCs have both digital and analog switch capacitor blocks. Verify that the same clock is selected for both analog and digital blocks.
- **Clock Range**: There are minimum and maximum clock rates for each of the analog user modules that are based on the analog SC blocks. Verify that the selected clock is within the specified clock range. Remember that the actual SC clock frequency is one forth the input clock frequency.
- **Clock Phase**: When a signal flows from one SC block-based user module to another, the clock phases may need to be reversed. Most user-modules that use a SC block will have a ClockPhase parameter. Make sure a signal path that goes through two or more SC blocks alternate between **Normal** and **Swapped**.
- **Power Settings**: Power settings for user modules that contain SC blocks need to be set relative to the speed of the analog clock. For high clock rates, the power setting of the SC blocks also need to be set high.

- **Reference Mux**: Because the Reference Mux is global, all analog SC block-based components should share the same setting. Verify that all analog components are compatible with the selected Ref Mux setting.
- **Interrupts**: Most of the ADCs require some processing in the ISR (Interrupt Service Routine). Verify that the specific ADC interrupt and the global interrupts are enabled.
- **CPU Overhead**: ADCs that process the results in the ISR can consume a large percentage of the total CPU cycles when operating at high speeds. If other components also require interrupts, you may need to reduce the sample rate.

Summary

Understanding the basic PSoC 1 analog architecture can help you understand the global analog parameters and the individual analog user module parameters. The global Ref Mux setting and how the references are generated is probably the most important part of the architecture. Although the broad range of reference settings may seem confusing at first, they provide one of the most flexible analog systems in a mixed signal microcontroller available in the market today.

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